6SN7 – LINE STAGE

Push-Pull Balanced Transformer Coupled Line Stage

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1.0 Introduction.

This line stage was designed as a companion for the KT88 (triode) mono-block power amplifiers. The output is in balanced format, connected to each power amplifier using XLR connectors. It can accept both either balanced and unbalanced inputs. The balanced input format is provided specifically to accept the signal from a CD player which I equipped with the Sowter type 8347 DAC signal transformers. This transformer provides an elegant solution to the issue of elimination of all silicon elements from the analogue signal path of a CD source. (When connected per the manufacturer's recommendations, the transformer will provide a balanced output of 473Vpk if the D-A output is 1.2mApk.)

2.0 Design Description.

A 6SN7 long-tailed-pair is connected as a Class A push-pull stage using the Lundahl 1660 PP interstage transformer. The secondaries are configured so as to provide a 2.25+2.25 : 1+1 step-down. To minimise squarewave overshoot, a 4.02k resistance is placed in parallel with each secondary phase. The plate resistance of a 6SN7 at the operating point is approximately 7.2kΩ. This is reduced by the square of the step-down ratio, 5.06 thus the impedance at each secondary is 1.42kΩ. This is in parallel with 4.02kΩ resulting in an output impedance for each phase of 1.05kΩ. An advantage of the transformer coupled output is that it permits isolation. The secondary centre-tap is shown not grounded at the line stage, rather at the power amplifier end. This eliminates the possibility of ground loop inteference.

The tail is returned to –175V via an 11kΩ resistance while the transformer primary centre-tap is supply with a B+ at 185V. Both grids are referenced to ground using 681kΩ leak resistors. The inputs are selected using a Elma 4 pole rotary switch. For unbalanced inputs, the –phase grid is grounded by the switch. The volume control design is a little unusual. I had experimented with connecting a volume control potentiometer as a variable shunt to ground, the pass signal being attenuated using a series resistance. In this way, the 'pass' signal is connected directly and not via the potentiometer wiper. Even using high quality Alps potentiometers, this technique results in a readily discernible improvement in clarity. By providing an equal value resistance in both phases of the balanced inputs, the potentiometer can by used as a variable cancellation shunt between the phases thereby eliminating the need for four matched potentiometers in a stereo balanced line-stage. The choice of series resistance value needs a little thought. First, it must be high enough in value such that when the shunt is approaching zero, the load presented is acceptable to all sources which are to be used. Second, it must be small enough in value that the HF roll-off resulting by it acting in combination with the Miller capacitance of the 6SN7 is acceptable. The value of 51.1kΩ results in an HF pole at the plate far above that due to the interstage transformer. This is due in part to the rising load reactance presented to the plate with frequency by the transformer. In designing source line output stages, I aim to keep the source impedance below 5kΩ. Taking the transformer coupled DAC as an example: The I/V resistance is 25Ω while the step-up is 1:18.7 resulting in an impedance transformation of 1:350 and thus a reflected secondary impedance of 8.74kΩ. This is in parallel with a 47kΩ resistor placed across the secondary (per Sowter recommendation) giving a balanced source impedance of 7.4kΩ or 1.84kΩ for each phase. In balanced input mode, the minimum load presented is 2 X 51.1kΩ, thus significantly greater than 10X the source impedance.

3.0 Measured Performance of the Line Stage.

SMPTE Intermodulation Distortion using unbalanced input (60Hz / 7kHz mixed 4:1):
(The IMD measurements were taken using a Heathkit IM-5248 analyzer.)

0.3Vrms	0.028%
1Vrms	0.012%
3Vrms	0.039%

THD:
(The THD measurements were taken using HP339a analyzer.)

	100Hz	1kHz	5kHz
.1Vrms	0.047%	0.035%	0.081%
.3Vrms	0.015%	0.012%	0.026%
1Vrms	0.03%	0.0065%	0.01%
3Vrms	0.035%	0.016%	0.015%

Bandwidth:

-1dB	18Hz to 20kHz
-3dB	<10Hz to 38kHz

Voltage gain:	12.3dB balanced in to balanced out
Input impedance (Minimum):	56kΩ, unbalanced; 112kΩ, balanced
Signal to noise ratio:	82dB unweighted (referred to 1.6Vrms)

NOTE: These measurements reflect the 'least good' channel. An interesting point is that both the IMD and the THD increase at lower signal levels. Previously, I had encountered the same behaviour while breadboarding a similar circuit using push-pull interstage transformers. I suspect that this is due to the B-H "kink" about the zero becoming an increasingly large percentage of a small signal.

4.0 Power Supply.

I used an adapted surplus regulated power supply. 360V from the supply is biased to 175V below ground and 185V above ground using one 100V and one 75V zener diode. Theses diodes do not have to support any significant current draw because the ground rail thus created is simply acting as a bias voltage source for the 6SN7 grids. The zener bias current is developed using a 1W / 82.5k resistor between ground and +185V for a bias current of 2mA. A design for a suitable regulated supply is shown. While a well filtered unregulated supply is also suitable, I have a strong preference for regulation because, amongst other things, it minimizes the impact of the antics of the utility company on the performance of my system! The suggested power supply uses a standard Hammond transformer. Low noise hexfred diodes are specified to rectify the AC. The peak voltage is developed across C1. R1 serves to limit the peak rectification current. The regulator uses the pentode section of a 6BM8 for the series regulator element to handle the total current of 33mA. The screen grid supply is further filtered by R2 and C2, this point also serving as the B+ supply to the error amplifier. The use of a pentode with the screen grid filter shown increases ripple rejection by approximately 27dB as compared to the use of a triode. This makes the use of a π DC input filter unneccesary. The triode section having a μ of 70 serves well for the error amplifier. Two 100V zener diodes provide the reference voltage. The zener diodes are biased at 2mA by the error amplifier plate current. The power supply is bypassed at the line-stage with a 10μF film capacitor across the zener string and a 20μF film capacitor across the 360V points.

5.0 DC Heater Supply.

The two 6SN7 heater are connected in series to permit the simple application of a 12V regulator. The raw DC is developed using a voltage doubler from a 5V winding. Note that the current capacity of the winding has to be 2.8 times that drawn by the load. The 6SN7s are connected in series and thus the current the winding has to support is 1.68A. The DC is regulated at 12V using a 7812 regulator mounted on a heatsink. 5V in my experience is a little marginal with respect to drop-out of the 7812. It is important therefore, to combine the large capacitors specified with the low forward drop of the 1N5822 Schottky diodes. The use of Schottky diodes will help to mitigate the noise resulting from the high charging currents. Additionally, 2.7Ω / 1μF Zobel network is placed across the output of the regulator to enhance RF rejection. Note, if you place the regulator away from DC source, it is a good idea to include a further 1000μF capacitor, located within two inches of the regulator.

6.0 Construction.

Interstage transformers are susceptible to induced hum from power transformers and wiring carrying heavy ripple currents. The sensitivity of the open frame Lundahl transformer is accentuated by the location of the transformer at a low signal level stage. For this reason, I strongly recommend that you use a separate chassis for both the B+ and heater supplies. This recommendation includes the heater regulator. (I installed mine inside the line stage chassis since there was not room inside the adapted surplus power supply. I found it necessary to add pre-filtering (2Ω and 10,000μF) to reduce the ripple on the incoming DC to a level that did not affect the nearby interstage transformer.) If you do not wish to do this then at least use a toriodal power transformer with a rating well in excess of the power requirement, 25W. This is to ensure that the toroid cannot saturate. While the stray field of a toroid operating within the rating is very low, the efficiency of the toroidal core causes abrupt onset of saturation if it is over-run, in which case the leakage field is very pronounced. Such over-run may not be obvious when considering rms current requirements only. It is necessary also to ensure that the peak rectification currents will not saturate the core causing bursts of noise at at 1/120sec intervals. I would suggest a unit rated at least for 60VA.

I used a Neutrik 4 pin connector to interface the line stage umbilical to the power supply.

SAFETY: Allow a minimum of three mintues for the polypropylene capacitors to bleed down via the bleed resistors. DO NOT WORK on the circuits without REMOVING THE LINE CORD FROM THE IEC RECEPTACLE & waiting for at least three minutes. Use a voltmeter to check that the CAPACITORS HAVE DISCHARGED.

The author cannot accept responsibility for your ability or otherwise to work safely with the high voltages present in vacuum tube circuits.